Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTION:**

1. **B0**
2. **B2**
3. **Bn**
4. **B3**
5. **B1**
6. **NE**
7. **VEE**
8. **GND**
9. **S1**
10. **S0**
11. **A3**
12. **A0**
13. **An**
14. **A1**
15. **A2**
16. **VCC**

**.080”**

**.070”**

**2 1 16 15**

**6 7 8 9 10**

**14**

**13**

**12**

**11**

**3**

**4**

**5**

**MASK  
REF**

**11703B**

**HC**

**Top Material: Al**

**Backside Material: Si Ni2**

**Bond Pad Size: .004” X .004”**

**Backside Potential: Isolated**

**Mask Ref: 11703B**

**APPROVED BY: DK DIE SIZE .070” X .080” DATE: 12/19/17**

**MFG: RCA/HARRIS THICKNESS .020” P/N: 54HC4052**

**DG 10.1.2**

#### Rev B, 7/1